

What is Claimed is:

- 1        1. A comparator unit comprising:
  - 2            a first comparator responsive to a first signal group,
  - 3            the first comparator determining when a first predetermined
  - 4            relation is present to a first reference signal group;
  - 5            a second comparator responsive to a second signal
  - 6            group, the second comparator determining when a second
  - 7            predetermined relation is present to a second reference
  - 8            signal group; and
- 9            a second inter-comparator conductor, the second inter-
- 10          comparator conductor applying an indicia of an
- 11          identification of the second predetermined condition to
- 12          first comparator, the first comparator generating an event
- 13          signal when the first and the second predetermined
- 14          conditions are identified.
- 15
- 16        2. The comparator unit as recited in claim 1 wherein
- 17        the first and the second signal groups are the same.
- 18
- 19        3. The comparator unit as recited in claim 1 wherein
- 20        the first and second signal groups are address signal
- 21        groups.
- 22
- 23        4. The comparator unit as recited in claim 1 wherein
- 24        the first and the second signal groups are same address
- 25        signal group.

1

2       5. The comparator unit as recited in claim 1 wherein  
3 either one of the first and the second comparator can  
4 generate an event signal when at least one of a touching  
5 requirement and an exact requirement is satisfied by an  
6 applied address signal group.

7

8       6. A comparator unit comprising:  
9           a first comparator and a second comparator, each  
10          comparator including:

11            a comparison logic unit for comparing an input  
12          signal group with a predetermined condition is identified;  
13          and

14            an event signal generating unit, the comparison  
15          logic unit applying a signal to the event generator unit  
16          and to the event signal generating unit of the other  
17          comparator when the predetermined condition is identified,  
18          the event generating unit generating an event signal when  
19          the signals from the two comparator logics have  
20          predetermined values.

21

22       7. The comparator unit as recited in claim 6 wherein  
23          each comparator includes a data qualifying unit, the data  
24          qualifying unit responsive to an input signal, the input  
25          signal determining when a preestablished signal group has  
26          certain characteristics, the data qualifying unit applying

1 a control signal to the comparison logic unit determining  
2 whether generation of an event signal is enabled.

3

4       8. The comparator unit as recited in claim 6 wherein  
5 the input signal groups are address signal groups, the  
6 predetermined conditions each reference an address signal  
7 group.

8

9       9. The comparator unit as recited in claim 8 wherein  
10 the address signal groups are the same signal group.

11

12      10. The comparator unit as recited in claim 6 wherein  
13 the predetermined conditions are entered in the comparator  
14 logic by control signals.

15

16      11. The comparator as recited in claim 10 wherein  
17 each comparator can operate independently, each comparator  
18 capable of generating an event signal in response to at  
19 least one of a touching requirement and an exact  
20 requirement.

21

22      12. The method of determining when a first and a  
23 second input signal group meets at least one predetermined  
24 condition, the method comprising:

25       determining in a first comparator when the first input  
26 signal group meets a first predetermined condition;

1       determining in a second comparator when the second  
2 input signal group meets a second predetermined condition;  
3 and

4       generating an output signal when the first and the  
5 second predetermined conditions are met.

6

7       13. The method as recited in claim 12 wherein the  
8 first and the second input signal group are different  
9 address signal groups.

10

11       14. The method as recited in claim 12 wherein the  
12 first and the second input signal groups are the same  
13 address signal group.

14

15       15. The method as recited in claim 12 wherein the at  
16 least one predetermined condition is selected from the  
17 group consisting of a touching requirement and an exact  
18 requirement.

19

20       16. The method as recited in claim 12 further  
21 comprising applying a signal to the comparators indicative  
22 an associated signal group characteristic, the signal  
23 controlling generation of the output signal.

24

25       17. In a target processor, apparatus for generating a  
26 trigger signal, the apparatus comprising:

1           a plurality of event signal generating units, wherein  
2 at least one signal generating unit is a comparator unit,  
3 the comparator unit including:

4           a first comparator and a second comparator, each  
5 comparator having:

6           a comparison logic unit for comparing an  
7 input signal group with a predetermined condition is  
8 identified; and

9           an event signal generating unit, the  
10 comparison logic unit applying a signal to the event  
11 generator unit and to the event signal generating unit of  
12 the other comparator when the predetermined condition is  
13 identified, the event generating unit generating an event  
14 signal when the signals from the two comparator logics have  
15 predetermined values.

16           a trigger generation unit coupled to the plurality of  
17 event signal generation units, the trigger generation unit  
18 responsive to at least one preselected event signal for  
19 generating an associated trigger signal, the trigger  
20 generating unit generating a trigger control signal;

21

22           18. The target processor as recited in claim 17  
23 wherein the comparator unit receives a program counter  
24 address input signal.

25

26           19. The target processor as recited in claim 17  
27 wherein one comparator receives a program counter address  
28 counter address input signal and the second comparator

1 received an address signal group referenced the program  
2 counter address.

3

4 20. The target processor as recited in claim 17  
5 wherein the preselected condition is selected from the  
6 group consisting of a touching requirement and an exact  
7 requirement.